

Application No.: 10/724,277

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Docket No.: 188122001500

**AMENDMENTS TO THE SPECIFICATION**

Please replace the first paragraph with the following amended paragraph.

[0001] This application is a continuation application and claims the benefit of co-pending U.S. application no. 10/713,729, "System And Method For Dynamically Compressing Circuit Components During Simulation," filed November 13, 2003. This application is also related to the following applications: System And Method For Adaptive Partitioning Of Circuit Components During Simulation, U.S. application no. 10/713,751; System And Method For Communicating Simulation Solutions Between Circuit Components In A Hierarchical Data Structure, U.S. application no. 10/713,754; System And Method For Supporting Multi-rate Simulation Of A Circuit Having Hierarchical Data Structure, U.S. application no. 10/713,753; and System And Method For Dynamically Representing Repetitive Loads Of A Circuit During Simulation, U.S. application no. 10/713,728; all of which are assigned to Cadence Design Systems, Inc. and all of which are incorporated herein in their entirety by reference.

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